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A Parallel Preconditioning Strategy for Efficient Transistor-Level Circuit Simulation

David M. Day

Applied Mathematics & Application

Sandia National Laboratories

Albuquerque, NM 87185-1320

dmday@sandia.gov

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H. Thornquist, E. Keiter, R.J. Hoekstra

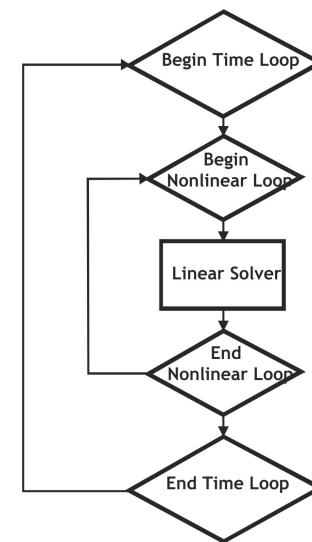
Electrical and Microsystems Modeling Department

E. G. Boman

Scalable Algorithms Department

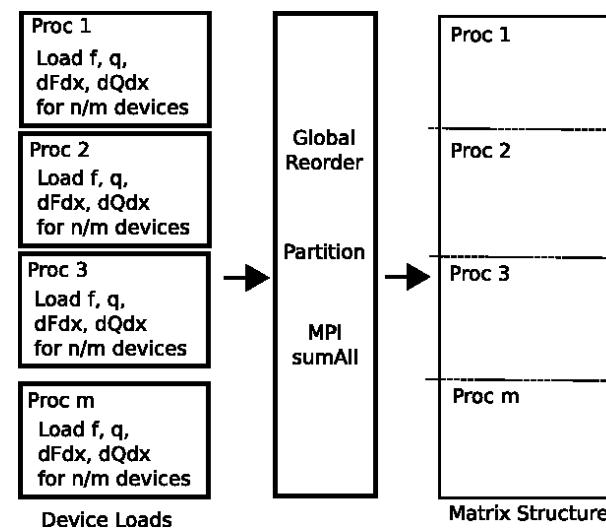
- Differential algebraic equation, $f(x(t)) + \frac{dq(x(t))}{dt} = b(t)$
- Transient simulation: $(G + Q/\delta t)\delta x = b - f - q/\delta t$
- Inductance $G(t) = \frac{df}{dx}(x(t))$, Capacitance $C(t) = \frac{dq}{dx}(x(t))$
- Initial DC operating point: $f(x_o) = 0, G \delta x = -f(x_o)$

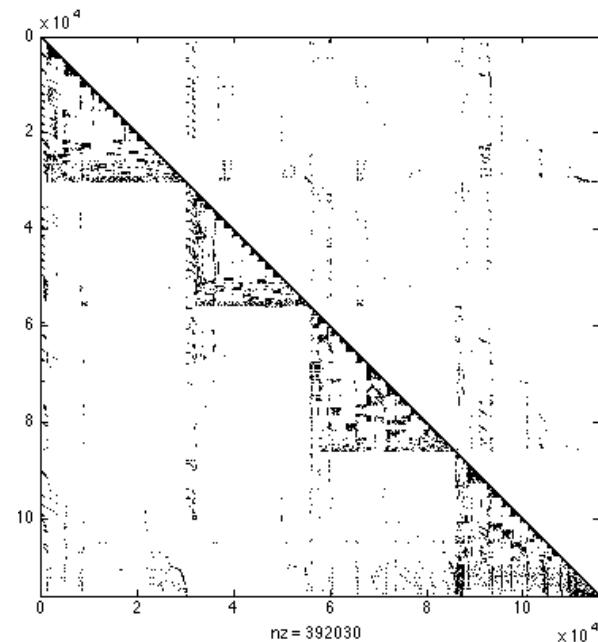
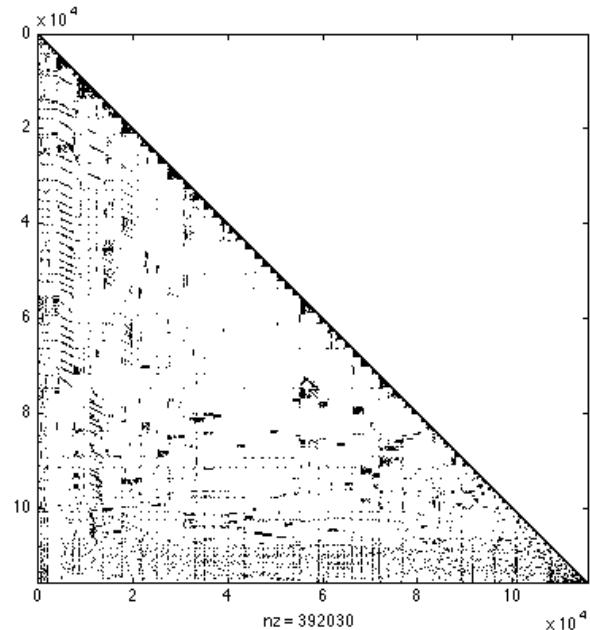
$G + C$, many time steps,
sparse linear systems,
weighted bipartite graphs,
Solver structure



parasitic extraction, full systems,
bottleneck, parallel computing,
graph partitioning

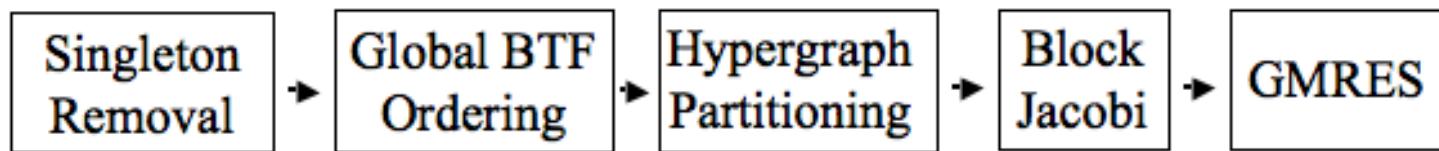
Separate partitions
for device load
and linear solve

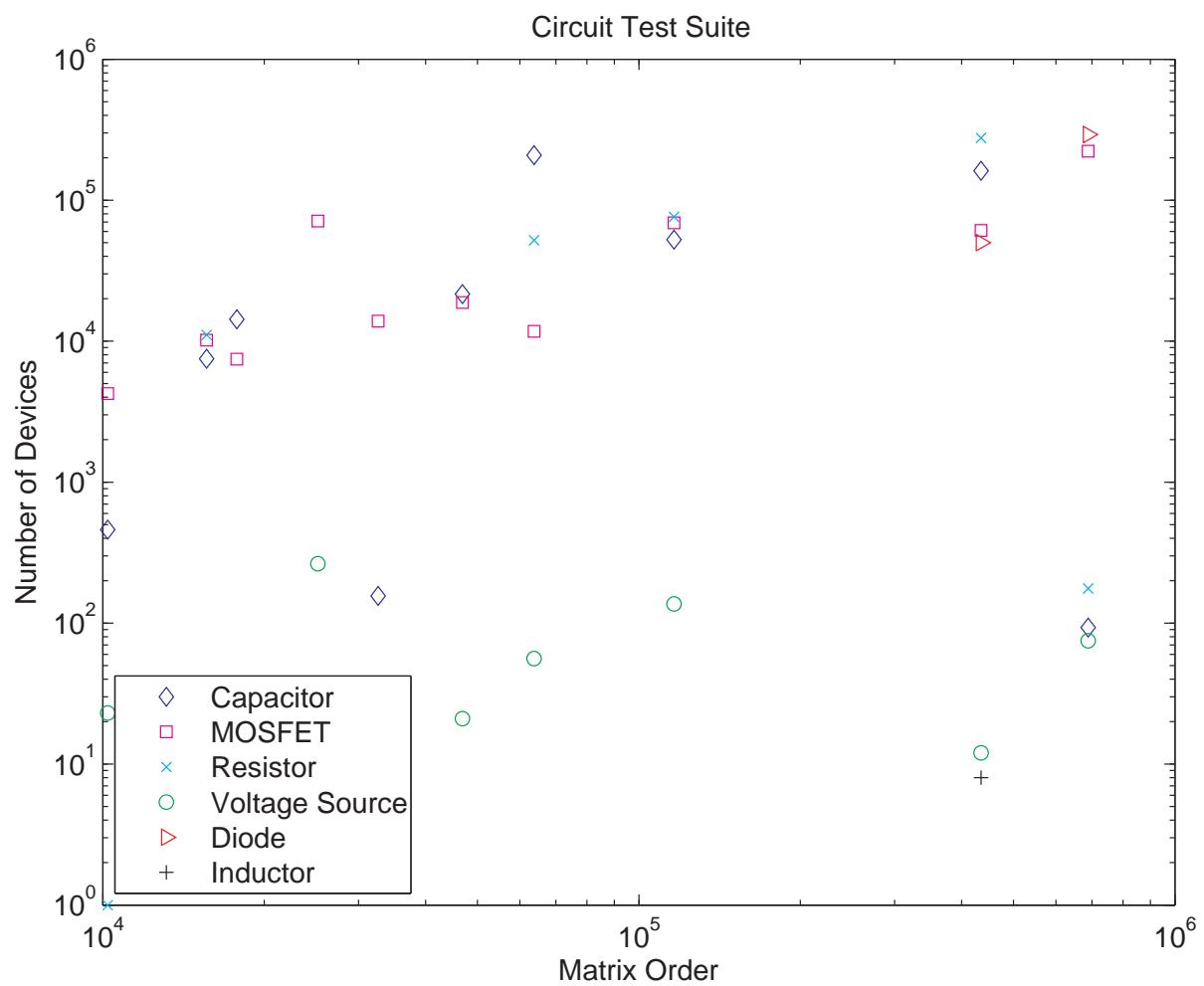




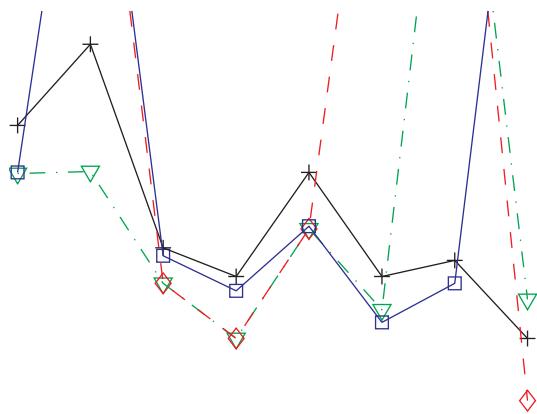
G for ckt3 before and after hypergraph partitioning

New Linear Solution Strategy

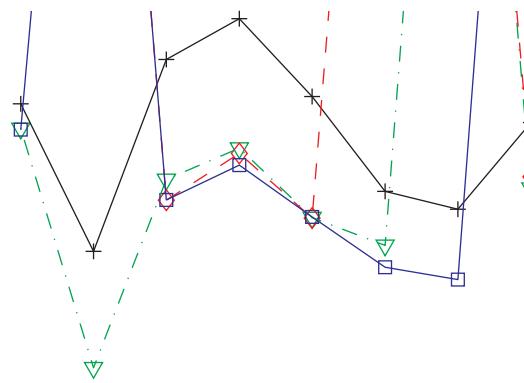




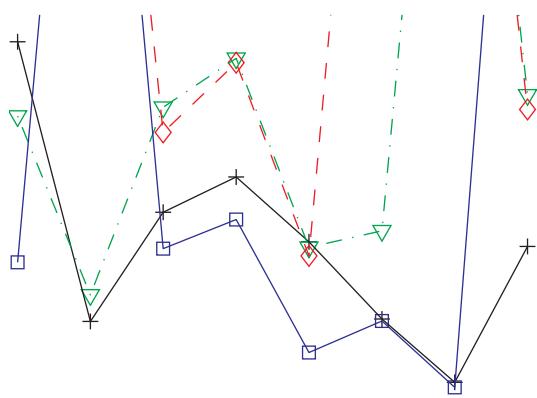
Setup



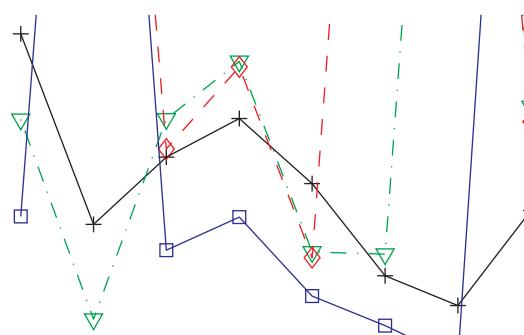
Load



Solve

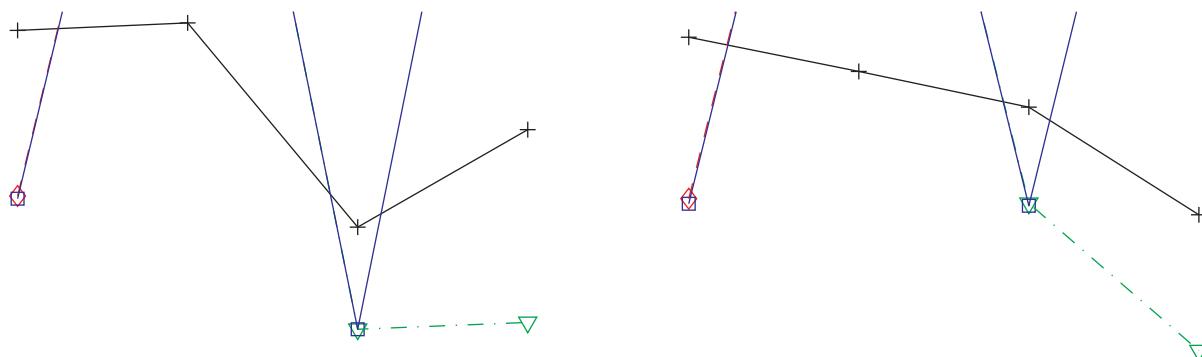


Total

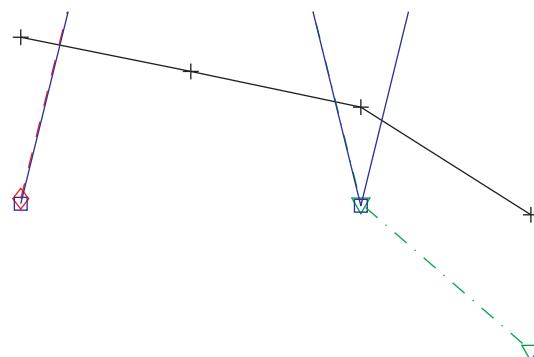


+ KLU, v SuperLU, diamond DD, box BTF

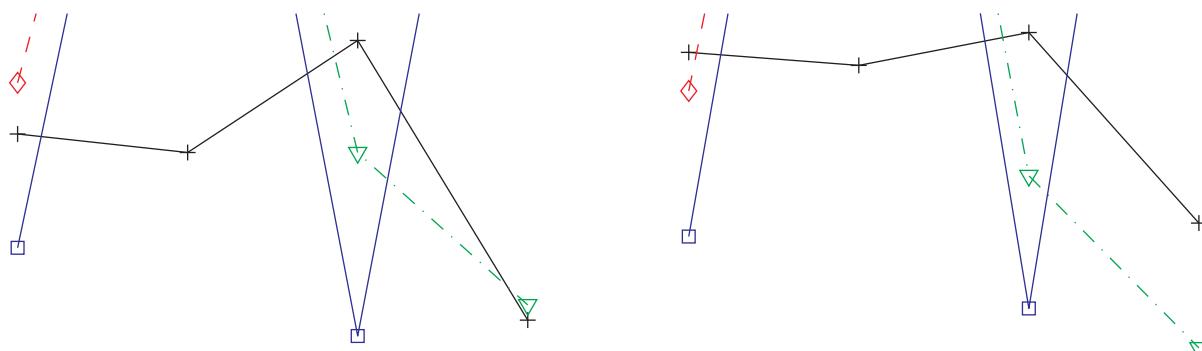
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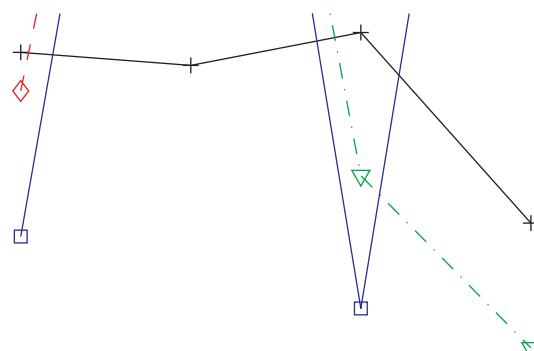
Load



Solve



Total



+ KLU, v SuperLU, diamond DD, box BTF

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